Sierra Components, Inc.

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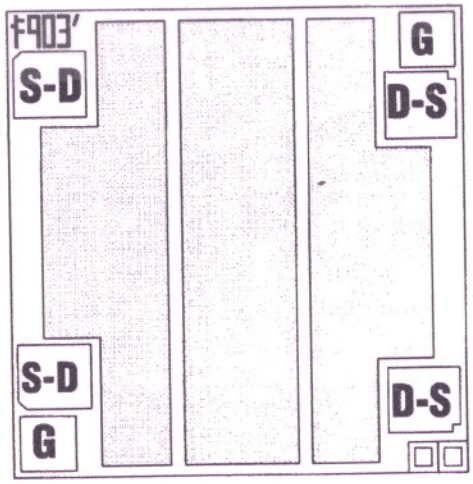
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Die Size = 0.040" X 0.040"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ903 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	−25	−40		V	$I_G = -1\ \mu A$, $V_{DS} = ØV$	
Reverse Gate Leakage Current	I_{GSS}		−0.1	−1	nA	$V_{GS} = -15V$, $V_{DS} = ØV$	
Drain Saturation Current (Pulsed)	I_{DSS}	100		900	mA	$V_{DS} = 10V$, $V_{GS} = ØV$	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	−2		−7	V	$V_{DS} = 10V$, $I_D = 1\ nA$	
Dynamic Electrical Characteristics							
Drain Source ON Resistance	$r_{ds(on)}$		5		Ω	$I_D = 1\ mA$, $V_{GS} = Ø$	f = 1 kHz
Input Capacitance	C_{iss}		45		pF	$V_{DS} = ØV$, $V_{GS} = -10V$	f = 1 MHz
Feedback Capacitance	C_{iss}		22		pF	$V_{DS} = ØV$, $V_{GS} = -10V$	f = 1 MHz
Turn On Delay Time	$t_{d(on)}$		7		ns	$V_{DD} = 1.5V$, $I_{D(ON)} = 30\ mA$ $R_L = 50\Omega$, $V_{GS(ON)} = ØV$ $V_{GS(OFF)} = -7V$	
Rise Time	t_r		1		ns		
Turn Off Delay Time	$t_{d(off)}$		12		ns		
Fall Time	t_f		2		ns		

APPROVED BY: MG **DIE SIZE : 40 x 40 Mils** **DATE: 5/30/12**

MFG: Inter-FET **THICKNESS:** **P/N: IFN5434/2N5434**